AF/2814

PATENT
Attorney Docket No.2987.2US (96-790.1)

NOTICE OF EXPRESS MAILING

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Serial No.:	09/526,814	Group Art Unit No.:	2814
Filing date:	March 16, 2000	Examiner:	N. Ha
For (title):	METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE		

TRANSMITTAL OF APPEAL BRIEF (PATENT APPLICATION — 37 C.F.R. § 192)

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on November 15, 2001.

2. STATUS OF APPLICATION
This application is on behalf of
- [X] other than a small entity
- [ ] small entity

verified statement:
- [ ] attached
- [ ] already filed

3. FEE FOR FILING APPEAL BRIEF
Pursuant to 37 C.F.R. § 1.17(f) the fee for filing the Appeal Brief is:

[ ]	small entity status	$155
[X]	other than a small entity	$320

4. EXTENSION OF TIME

[ ] A petition for Extension of Time for a month extension of time for filing the Appeal Brief is enclosed.

5. FEE PAYMENT

[X] Check No. 1651 is enclosed in payment of the fee for filing the Appeal Brief plus any extension of time for which a petition has been filed.
[ ] Please charge this fee to deposit account No. 20-1469 (a duplicate copy of this notice is enclosed--see below).

Any additional appeal fees which are not otherwise submitted herewith or which are insufficient should be charged to deposit account no. 20-1469. A duplicate copy of this notice is enclosed. Please address all communications in connection with this appeal to the address indicated below.

Respectfully submitted,

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Date: January 10, 2002
Enclosures: As identified above
BBJ/djp

PATENT

#10/GB
1-23-02
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Michael B. Ball

Serial No.: 09/526,814

Filed: March 16, 2000

For: METHOD AND APPARATUS FOR ROUTING DIE INTERCONNECTIONS USING INTERMEDIATE CONNECTION ELEMENTS SECURED TO THE DIE FACE

Examiner: N. Ha

Group Art Unit: 2814

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BRIEF ON APPEAL

Assistant Commissioner for Patents
Washington, D.C. 20231

Attn: Board of Patent Appeals and Interferences

Sirs:

This brief is submitted in triplicate and in the format of 37 C.F.R. § 1.192(c). A check in the amount of $320.00 for the fee under 37 C.F.R § 1.17(c) for filing a brief in support of an appeal is enclosed.

(1) REAL PARTY IN INTEREST

The real party in interest in the present pending appeal is Micron Technology, Inc., assignee of the pending application as recorded with the United States Patent and Trademark Office on Feb. 14, 1997, Reel 8437, Frame 0525.

(2) RELATED APPEALS AND INTERFERENCES

Neither the Appellant, the Appellant's representative nor the assignee is aware of any pending appeal or interference which would directly affect, be directly affected by or have any bearing on the Board's decision in the present pending appeal.

(3) STATUS OF THE CLAIMS

Claims 1 through 4 and 15 through 25 are pending in the application.

Claims 5 through 14 have been canceled.

Claims 1 through 4, and 15 through 25 stand rejected.

Claims 1 through 4, and 15 through 25 are the subject of the present pending appeal.

(4) STATUS OF AMENDMENTS

An amendment to claim 1 was proposed by Applicant subsequent final rejection. In an Advisory Action mailed Nov. 2, 2001 the Examiner stated that the amendment would be entered for purposes of appeal. The claims as presented in Appendix A, attached hereto, reflect entry of the amendment as indicated in the Advisory Action mailed Nov. 2, 2001.

(5) SUMMARY OF THE INVENTION

The presently claimed invention is directed to an apparatus for routing die interconnections which uses intermediate connection elements as well as semiconductor devices utilizing such an apparatus. FIGS. 2A and 2B show a semiconductor device 30 which incorporates the inventive apparatus. The semiconductor device 30 includes a plurality of peripheral bond pads 116. A sheet-like insulating layer, film or tape segment 32 is disposed on an active surface 114 of the semiconductor device 30. An exemplar material used to form the sheet like-like insulating layer 32 includes a polyimide film, such as Kapton®. (Specification, page 8, lines 24-30)

A plurality of contacts or jumper pads 120 are formed in or on the surface of the of the sheet-like insulating layer 32. As can be seen in FIG. 2B, the jumper pads are thus insulated on their respective die facing surfaces by means of the sheet-like insulating layer. (Specification page 8, lines 26-27 and page 9, lines 2 through 4). Such an embodiment insulates the jumper pads from any internal circuitry near the active surface of the die and thus protects such internal circuitry from interference or shorting which may be otherwise generated by the presence of the jumper pads or connections to the jumper pads as described below. (Specification, page 5, line 28 through page 6, line 3).

As seen in FIG. 4, conductors, shown as wire bonds 80, 81, 82, 83 and 84, may be used to electrically couple the jumper pads (labeled 320 in FIG. 4) with peripheral bond pads 316 which are in turn coupled with individual leads 66 of a lead frame. Additionally, conductors allow electrical coupling of one jumper pad 120, 320 to another. The jumper pads 120, 320 provide

multiple potential electrical pathways thereby allowing considerable flexibility in configuring (or reconfiguring) the input/output connections of a semiconductor die. (Specification, page 10, line 23 through page 11, line 2).

FIGS. 3 and 3A show another apparatus for routing die interconnections which is referred to generally as an adapter 46. The adapter 46 is configured to mate with an active surface 214 and bond pads 216 of a semiconductor die 42. The adapter 46 includes a support structure 48 which may be formed of a sheet-like structure. Examples of sheet-like structures include, for example, Kapton® or other tape as used in tape automated bonding, ceramic, silicon, or FR-4 as is known in the art. Desirably, the sheet-like structure is formed of a material having a coefficient of thermal expansion substantially matching the coefficient of thermal expansion of the semiconductor die 42. (As-filed specification, page 9, lines 11-17)

The adapter 46 further includes a plurality of jumper pads 220, a plurality of first contact pads 50 on a top surface 52 of the support structure 48 and a plurality of second contacts pads 54 along a bottom surface 56 of the support structure 48. The second contact pads 54 are electrically coupled to the first contact pads 50 such as by conductive contacts or conductive vias 58 formed within the support structure 48. (Specification, page 9, lines 7-9, 17-22).

The second contact pads 54 are arranged to match an arrangement of contacts, such as bumped bond pads 216 of the semiconductor die 42. When the adapter 46 is secured to the semiconductor die 42 the plurality of second contact pads 54 mate with the bumped pads 216. (Specification, page 9, lines 22-25). Again, conductors may be used to couple the various first contacts 50 with various jumper pads 220 allowing the input/output configuration of a given

semiconductor die 42 to be modified as desired.

As shown in FIG. 3A, any of the first contact pads 50 and the jumper pads 220 may have bumped contacts 61 placed thereon for purposes of mounting the resulting device to another component such as a carrier substrate. (Specification , page 9, lines 25-29).

(6) ISSUES

A. Whether claims 1 through 4, 15 through 17 and 19 through 25 are patentable over U.S. Patent 5,757,078 to Matsuda et al. under 35 U.S.C. §102(e)

B. Whether claim 18 is patentable over U.S. Patent 5,757,078 to Matsuda et al. and U.S. Patent 4,712,129 to Orcutt.

(7) GROUPING OF CLAIMS

The grouping of the claims is as follows:

(A) With respect to issue A independent claims 1, 15 and 17 stand and fall independent of one another.

Claim 4 stands and falls with claim 1. Claim 2 stands but does not fall with claim 1. Claim 3 stands but does not fall with claim 1

Claims 18, 19 and 21 stand and fall with claim 15. Claim 16 stands but does not fall with claim 15. Claim 20 stands but does not fall with claim 15

Claims 22 through 25 stand and fall with claim 17.

(B) With respect to issue B claims 18 stands and falls on its own.

(8) ARGUMENT

STANDARD OF PATENTABILITY UNDER 35 U.S.C. § 103(a)

Applicant notes that a proper rejection of claims under 35 U.S.C. § 102(e) requires that each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference. Verdegaal Brothers v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Further, the identical invention must be shown in as complete detail as is contained in the claim. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). See also, M.P.E.P. § 2131. In view of these requirements, and the arguments set forth below, Applicant submits that the Office has not properly established the anticipation of the presently claimed invention.

Applicant further notes that a proper rejection of claims under 35 U.S.C. § 103(a) requires the Patent and Trademark Office (hereinafter "the Office") to first establish a *prima facie* case of obviousness. M.P.E.P. § 2142. The standard for establishing a *prima facie* case of obviousness is set forth in M.P.E.P. 706.02(j) where it states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or

references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

In view of these standards, and the arguments set forth below, Applicant respectfully submits that the Office has not established a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

A.1 PATENTABILITY OF CLAIMS 1 AND 4

In an Office Action mailed August 22, 2001, and made Final (hereinafter "the Final Action"), the Examiner rejected claims 1 and 4 as being unpatentable over U.S. Patent 5,757,078 to Matsuda et al. (hereinafter "Matsuda") under 35 U.S.C. §102(e)

Applicant submits that the 35 U.S.C. § 102(e) anticipation rejections of claims 1 and 4 are improper because Matsuda fails to teach every limitation set forth in claims 1 and 4 of the presently claimed invention.

Independent claim 1 of the presently claimed invention is directed to an apparatus for routing interconnections among bond pads on a semiconductor die. The apparatus includes a sheet like, non-conductive structure having a first surface and a second surface for attachment to a semiconductor die. A plurality of electrically conductive discrete pads are attached to the first surface of the sheet-like, nonconductive structure. The plurality of electrically conductive

discrete pads each include an electrical connect portion and a portion facing the first surface with each discrete pad being electrically isolated about its respective portion facing the first surface of the sheet-like nonconductive structure. In other words, the discrete pads are electrically insulated from direct contact with any circuitry which is formed in or below the sheet like, non-conductive structure and which is adjacent the discrete pads.

In the Final Action, the Examiner cites Matsuda as teaching all of the limitations of independent claim 1. Particularly, the Examiner points to FIGS. 1 and 2 of Matsuda and states that Matsuda discloses a semiconductor die including a sheet-like nonconductive structure (23) having a first surface, and a second surface for attachment to the semiconductor die (21); and a plurality of electrically conductive discrete pads each having an electrical connection portion and a portion facing the first surface, each being electrically isolated about the portion facing the first surface. (See the Final Action, page 2).

However, as set forth above, Applicant respectfully submits that Matsuda fails to disclose every element as set forth in independent claim 1. Particularly, Matsuda fails to disclose a plurality of electrically conductive discrete pads having an electrical connection portion and a portion facing the first surface of the sheet-like nonconductive structure, with *each discrete pad being electrically isolated about the portion facing the first surface.*

Matsuda is directed to a semiconductor device package. The package disclosed by Matsuda includes a semiconductor die (21) coupled with a plurality of insulating film layers (25a-25c) through means of an adhesive agent (23). Wiring patterns (29) are formed between each film layer and are electrically interconnected from one layer to another by way of

conductive vias. Thus, the semiconductor chip is electrically connected to a plurality of conductive bumps by means of the layered wiring patterns and conductive vias.

The conductive bumps (31) are not electrically isolated about their respective surface facing portions as they are each connected to a wiring pattern (29) by a conductive via. Additionally, the wiring patterns (29) may not be classified as being electrically isolated on their respective surface facing portions. Rather, each wiring pattern (29) is electrically coupled at its surface facing portion to either another wiring pattern (29), a conductive bump (31), or an electrode pad (22) of the semiconductor device (21). For example, Matsuda states:

> The wiring pattern 29 between the second and third insulating films 25b and 25c are connected to the wiring patterns 29 between the first and second insulating film 25a and 25b via the viahole wiring patterns provided in the second insulating film 25b. Conductive projections, namely, bumps 31 are formed on the third insulating film 25c as an outermost layer of the insulating layer 25 and electrically connected to the wiring pattens 29 between the second and third insulating films 25b and 25c. The bumps 31 are directly bonded onto a printed circuit board (not shown) or the like and a desired semiconductor device can be constructed. (Col. 4, line 63 through col. 5, line 7).

Thus, Matsuda clearly fails to teach that a *plurality of electrically conductive discrete pads have a portion facing a surface of a sheet-like nonconductive structure, wherein the*

discrete pads are electrically isolated about their respective die facing portions.

As such, Applicant respectfully submits that Matsuda fails to anticipate claim 1 of the presently claimed invention.

Applicant further submits that claim 4, which is dependent from claim 1 and thus inherently includes all of the limitations set forth in claim 1, is likewise patentable over Matsuda.

A.2 PATENTABILITY OF CLAIM 2

Claim 2 was rejected on the same grounds as expressed in section A.1 of the argument above with respect to claim 1. However, Applicant submits that claim 2 is separately patentable over claim 1 in view of the following arguments.

In addition to the reasons for patentability expressed in section A.1 of the argument above, claim 2 recites that the apparatus further comprises at least one conductor extending between at least two of said plurality of electrically conductive discrete pads, said at least one conductor including at least a portion external to said sheet-like nonconductive structure. Applicant submits that Matsuda fails to teach such subject matter.

Particularly, Matsuda fails to teach at least one conductor extending between at least two electrically conductive discrete pads which are configured as set forth in claim 1, wherein the at least one conductor includes at least a portion which is external to the sheet-like nonconductive structure.

Thus, Applicant submits that claim 2 is clearly not anticipated by Matsuda.

A.3 PATENTABILITY OF CLAIM 3

Claim 3 was rejected on the same grounds as expressed in section A.1 of the argument above with respect to claim 1. However, Applicant submits that claim 3 is separately patentable over claim 1 in view of the following arguments.

In addition to the reasons for patentability expressed in section A.1 of the argument above, claim 3 recites that the apparatus further comprises at least one conductor extending from at least one bond pad of said die to at least one of said plurality of electrically conductive discrete pads.

Applicant submits that Matsuda fails to teach a conductor extending from a bond pad of the die to a discrete pad which is electrically isolated about its surface facing portion. Rather, Matsuda teaches a bond pad of the die (referred to therein as a conductor 22) which is coupled with a conductive bump by means of multiple wiring patterns and conductive vias. As set forth above in section A.1, none of the wiring patterns or the conductive bumps are taught to be electrically isolated about their respective die facing portions as set forth in the presently claimed invention.

Thus, Applicant submits that claim 3 is clearly not anticipated by Matsuda.

A.4 PATENTABILITY OF CLAIMS 15, 19 AND 21

In the Final Action the Examiner rejected claims 15, 19 and 21 as being unpatentable over Matsuda under 35 U.S.C. §102(e)

Applicant submits that the 35 U.S.C. § 102(e) anticipation rejections of claims 15, 19 and

21 are improper because Matsuda fails to teach every limitation set forth in claims 15, 19 and 21 of the presently claimed invention.

Independent claim 15 is directed to a semiconductor device having a die, including a plurality of bond pads disposed on a surface thereof; an adapter having a first plurality of discrete electrical contacts on a first surface thereof with each being electrically connected to one of the plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, each of the second plurality of discrete electrical contacts having and electrical connection portion and a die facing portion and each being electrically isolated about the die facing portions, at least some of the second plurality of discrete electrical contacts being in electrical communication with the first plurality of discrete electrical contacts; and a plurality of conductive bumps, each extending from one of the second plurality of discrete electrical contacts.

The Examiner cites Matsuda, and particularly FIGS. 1 and 2, as teaching all of the limitations of claim 15 of the presently claimed invention, including an adapter having a first plurality of discrete electrical contacts on a first surface thereof. Applicant respectfully disagrees.

As set forth above in section A.1, Matsuda teaches a semiconductor device package which includes a semiconductor die coupled with multiple layers of an insulating film. Conductive bumps positioned on the outer most layer of insulating film are electrically connected with the semiconductor die through a plurality of wiring patterns and conductive vias. Neither the conductive bumps nor the wiring patterns are taught to be *electrically isolated about their respective die facing portions* as set forth in claim 15. Thus, Applicant submits that claim 15 is

not anticipated by Matsuda.

Applicant further submits that claims 19 and 21, which are dependent from claim 15 and thus inherently include all of the limitations set forth in claim 15, are likewise patentable over Matsuda.

A.5 PATENTABILITY OF CLAIM 16

Claim 16 was rejected on the same grounds as expressed in section A.4 of the argument above with respect to claim 15. However, Applicant submits that claim 16 is separately patentable over claim 15 in view of the following arguments.

In addition to the reasons for patentability expressed in section A.4 of the argument above, claim 16 recites that the apparatus further comprises a protective coating over at least a portion of said die, said plurality of conductive bumps being at least partially exposed through said protective coating. Applicant submits that Matsuda fails to teach such subject matter.

While the Examiner cites col. 4, line 27 through col. 5, line 65 as teaching the subject matter of claim 16, the Examiner does not point to, and Applicant fails to see, any specific passages teaching a protective coating over at least a portion of the die and through which the plurality of conductive bumps are partially exposed.

Thus, Applicant submits that claim 16 is clearly not anticipated by Matsuda.

A.6 PATENTABILITY OF CLAIM 20

Claim 20 was rejected on the same grounds as expressed in section A.4 of the argument above with respect to claim 15. However, Applicant submits that claim 20 is separately patentable over claim 15 in view of the following arguments.

In addition to the reasons for patentability expressed in section A.4 of the argument above, claim 20 (depending from claim 15 by way of claim 19) further recites that at least one of the second plurality of discrete electrical contacts is electrically isolated from the plurality of bond pads disposed on the first surface of the die.

Applicant submits that Matsuda fails to teach a discrete electrical contact on the adapter which is electrically isolated from the plurality of bond pads disposed on the first surface of the die. Nor has the Examiner cited any specific teaching of Matsuda regarding such subject matter.

Thus, Applicant submits that claim 20 is clearly patentable over Matsuda.

A.7 PATENTABILITY OF CLAIMS 17, 22 THROUGH 25

In the Final Action the Examiner rejected claims 17, 22, 23 and 25 as being unpatentable over Matsuda under 35 U.S.C. §102(e)

Applicant submits that the 35 U.S.C. § 102(e) anticipation rejections are improper because Matsuda fails to teach every limitation set forth in claims 17, 22, 23 and 25 of the presently claimed invention.

Independent claim 17 is directed to a semiconductor device. The semiconductor device includes a die having a plurality of bond pads disposed on a first surface thereof; and an adapter

having a first plurality of discrete electrical contacts on a first surface thereof, each being electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the at least some of said second plurality of discrete electrical contacts being electrically isolated about a die facing portion thereof, and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts.

The Examiner relies on Matsuda as teaching all of the limitations of claim 17 referring specifically to FIGS. 1 and 2, and particularly stating that Matsuda discloses an adapter at both ends of the structure in FIG. 1 which includes a first plurality of electrical contacts on a first surface thereof. However, Applicant submits that Matsuda fails to teach all of the limitations of claim 17.

As set forth above in section A.1 of the argument, Matsuda teaches a semiconductor device package which includes a semiconductor die coupled with multiple layers of an insulating film. Conductive bumps positioned on the outer most layer of insulating film are electrically connected with the semiconductor die through a plurality of wiring patterns and conductive vias. Neither the conductive bumps nor the wiring patterns are taught to be *electrically isolated about their respective die facing portions* as set forth in claim 17. Thus, Applicant submits that claim 17 is not anticipated by Matsuda.

Applicant further submits that claims 22 through 25, which are dependent from claim 17 and thus inherently include all of the limitations set forth in claim 17, are likewise patentable over Matsuda.

B.1 PATENTABILITY OF CLAIM 18

In the Final Action the Examiner rejected claims 18 as being unpatentable over Matsuda view of U.S. Patent No. 4,712,129 to Orcutt (hereinafter "Orcutt") under 35 U.S.C. § 103(a). Applicant respectfully traverses this rejection as hereinafter set forth.

Claim 18 of the presently claimed invention depends from claim 17. Claim 18 recites that the adapter set forth in claim 17 further comprises a material having a coefficient of thermal expansion substantially matching the coefficient of thermal expansion of the die. The Examiner cites Matsuda as teaching all the limitations of claim 17, and then cites Orcutt as teaching "that the texture and the die have similar TCE in order to prevent cracking between the die and the substrate." (Final Office Action, page 3). Further, the Examiner states that "it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the matching TCE of Orcutt's in Matsuda et al. in order to prevent the cracking between the die and the substrate." (*Id.*).

As addressed above in section A.7, Matsuda fails to teach or suggest all of the limitations of claim 17. Particularly, Matsuda fails to teach or suggest an adapter which includes *at least some of a second plurality of discrete electrical contacts which are electrically isolated about a die facing portion thereof.* Orcutt likewise fails to teach or suggest such subject matter. Thus,

the combination of Matsuda and Orcutt fail to teach or suggest all of the limitations of the presently claimed invention as set forth in claim 18.

Applicant, therefore, submits that claim 18 is clearly patentable over the cited references of Matsuda and Orcutt, either taken individually or in combination.

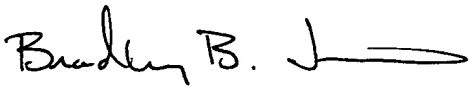
(9) APPENDIX

A copy of claims 1 through 4, and 15 through 25 is appended hereto as "Appendix A."

CONCLUSION

Applicant respectfully submits that claims 1 through 4, and 15 through 25 are allowable over the prior art relied upon and respectfully request that the rejections under 35 U.S.C. §102(e) and § 103(a) be reversed.

Respectfully submitted,



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APPENDIX A

1. An apparatus for routing interconnections among bond pads on a semiconductor die, comprising:

a sheet-like, nonconductive structure having a first surface, and a second surface for attachment to said semiconductor die; and

a plurality of electrically conductive discrete pads attached to said first surface, the plurality of electrically conductive discrete pads each having an electrical connect portion and a portion facing said first surface, each electrically conductive discrete pad of the plurality being electrically isolated about said portion facing said first surface.

2. The apparatus of claim 1, further comprising at least one conductor extending between at least two of said plurality of electrically conductive discrete pads, said at least one conductor including at least a portion external to said sheet-like nonconductive structure.

3. The apparatus of claim 1, further comprising at least one conductor extending from at least one bond pad of said die to at least one of said plurality of electrically conductive discrete pads.

4. The apparatus of claim 1, wherein said nonconductive structure is comprised of a dielectric film or sheet.

15. A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, each of said second plurality of discrete electrical contacts having an electrical connection portion and a die facing portion and each being electrically isolated about said die facing portions, at least some of said second plurality of discrete electrical contacts in electrical communication with said first plurality of discrete electrical contacts; and

a plurality of conductive bumps, each extending from one of said second plurality of discrete electrical contacts.

16. The semiconductor device of claim 15, further comprising a protective coating over at least a portion of said die, said plurality of conductive bumps being at least partially exposed through said protective coating.

17. A semiconductor device, comprising:

a die including a plurality of bond pads disposed on a first surface thereof;

an adapter having a first plurality of discrete electrical contacts on a first surface thereof, each electrically connected to one of said plurality of bond pads, and a second plurality of discrete electrical contacts on a second surface thereof, at least some of said second

plurality of discrete electrical contacts being horizontally remote from at least some of the plurality of bond pads disposed on the first surface of the die, the at least some of said second plurality of discrete electrical contacts being electrically isolated about a die facing portion thereof, and at least some other of said second plurality of discrete electrical contacts being electrically connected to said first plurality of discrete electrical contacts.

18. The semiconductor device of claim 15, wherein the adapter comprises a material having a coefficient of thermal expansion substantially matching a coefficient of thermal expansion of said die.

19. The semiconductor device of claim 15, wherein the adapter comprises at least one conductive via extending between at least one of the first plurality of discrete electrical contacts and at least one of the at least some other of said second plurality of discrete electrical contacts.

20. The semiconductor device of claim 19, wherein at least one of the second plurality of discrete electrical contacts is electrically isolated from the plurality of bond pads disposed on the first surface of the die.

21. The semiconductor device of claim 15, wherein the adapter is adhesively secured to the die.

22. The semiconductor device of claim 17, wherein the adapter is adhesively secured to the die.

23. The semiconductor device of claim 17, further comprising a plurality of conductive vias extending through said adapter electrically connecting said first plurality of discrete electrical contacts and the at least some other of the second plurality of discrete electrical contacts.

24. The semiconductor device of claim 17, wherein the adapter comprises a tape-like structure.

25. The semiconductor device of claim 17, wherein at least one of the second plurality of discrete electrical contacts is electrically interconnected with a second die.